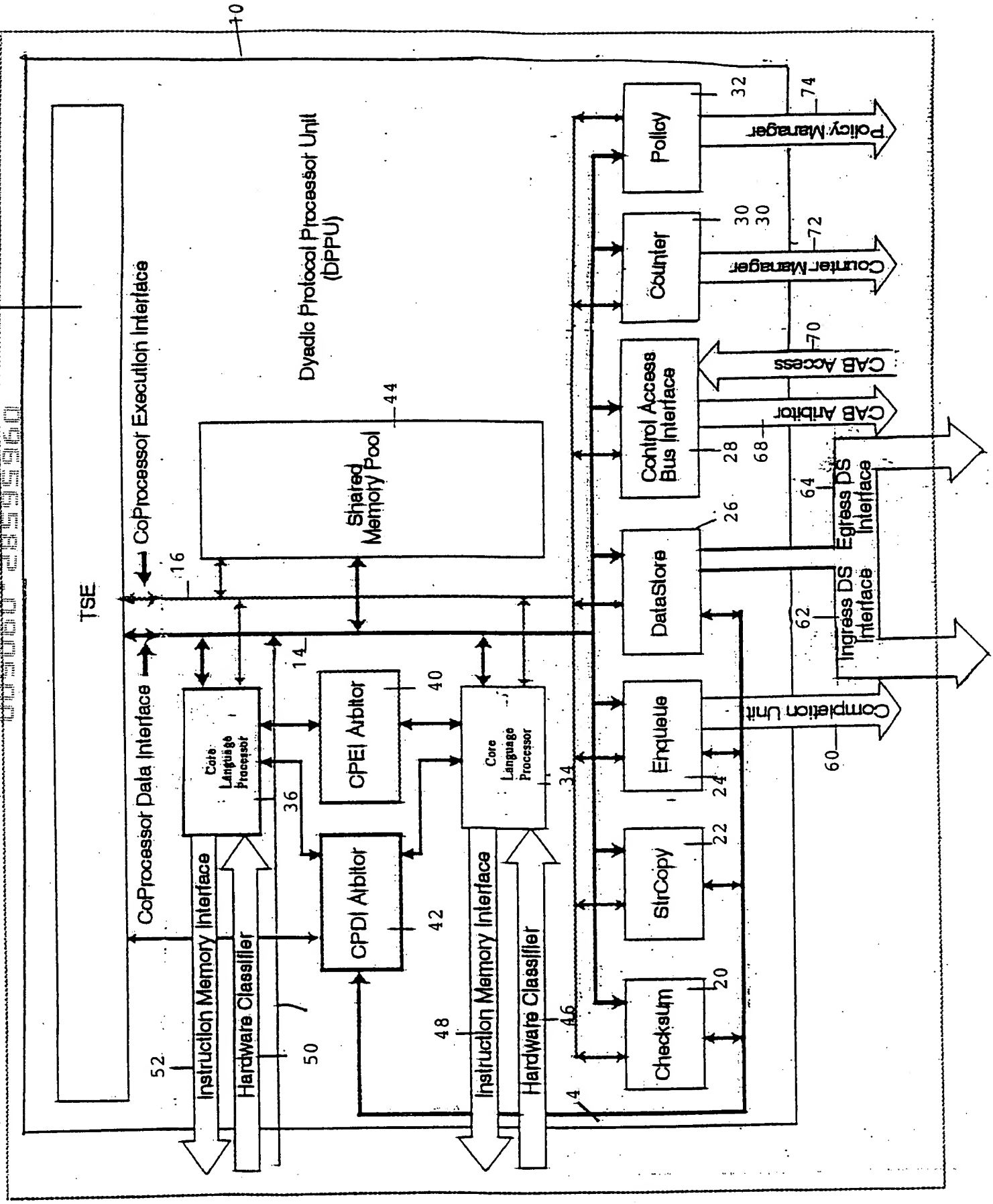
10
12
TSE
CoProcessor Execution Interface
Dyadic Protocol Processor Unit (DPPU)
Shared Memory Pool
44
16
CoProcessor Data Interface
14
Core Language Processor
36
CPEI Arbitor
40
CPDI Arbitor
42
Core Language Processor
34
Instruction Memory Interface
Hardware Classifier
52
50
48
Instruction Memory Interface
Hardware Classifier
46
4
Policy
32
74
Policy Manager
Counter
30
30
72
Counter Manager
Control Access Bus Interface
28
70
CAB Access
CAB Arbitor
68
64
Egress DS Interface
DataStore
26
62
Ingress DS Interface
Enqueue
24
Completion Unit
60
StrCopy
22
Checksum
20

FIGURE 1

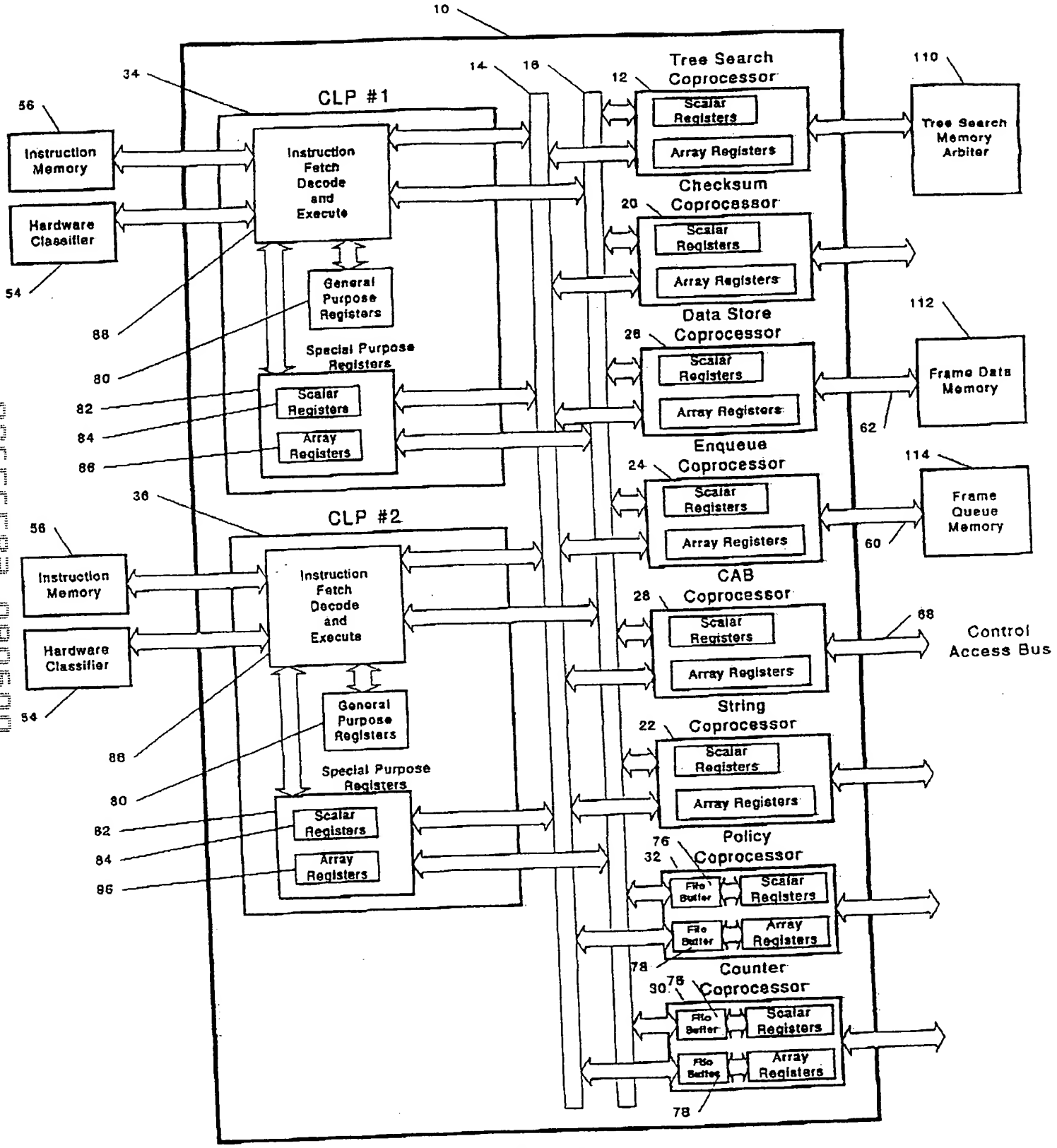
10
CLP #1
34
56
Instruction Memory
Hardware Classifier
54
Instruction Fetch Decode and Execute
General Purpose Registers
Special Purpose Registers
Scalar Registers
Array Registers
88
80
82
84
86
CLP #2
36
Tree Search Coprocessor
12
14
16
110
Tree Search Memory Arbiter
Checksum Coprocessor
20
Data Store Coprocessor
26
112
Frame Data Memory
62
Enqueue Coprocessor
24
114
Frame Queue Memory
60
CAB Coprocessor
28
68
Control Access Bus
String Coprocessor
22
Policy Coprocessor
76
32
File Buffer
Counter Coprocessor
30
78
US-09-680,500

Figure 2

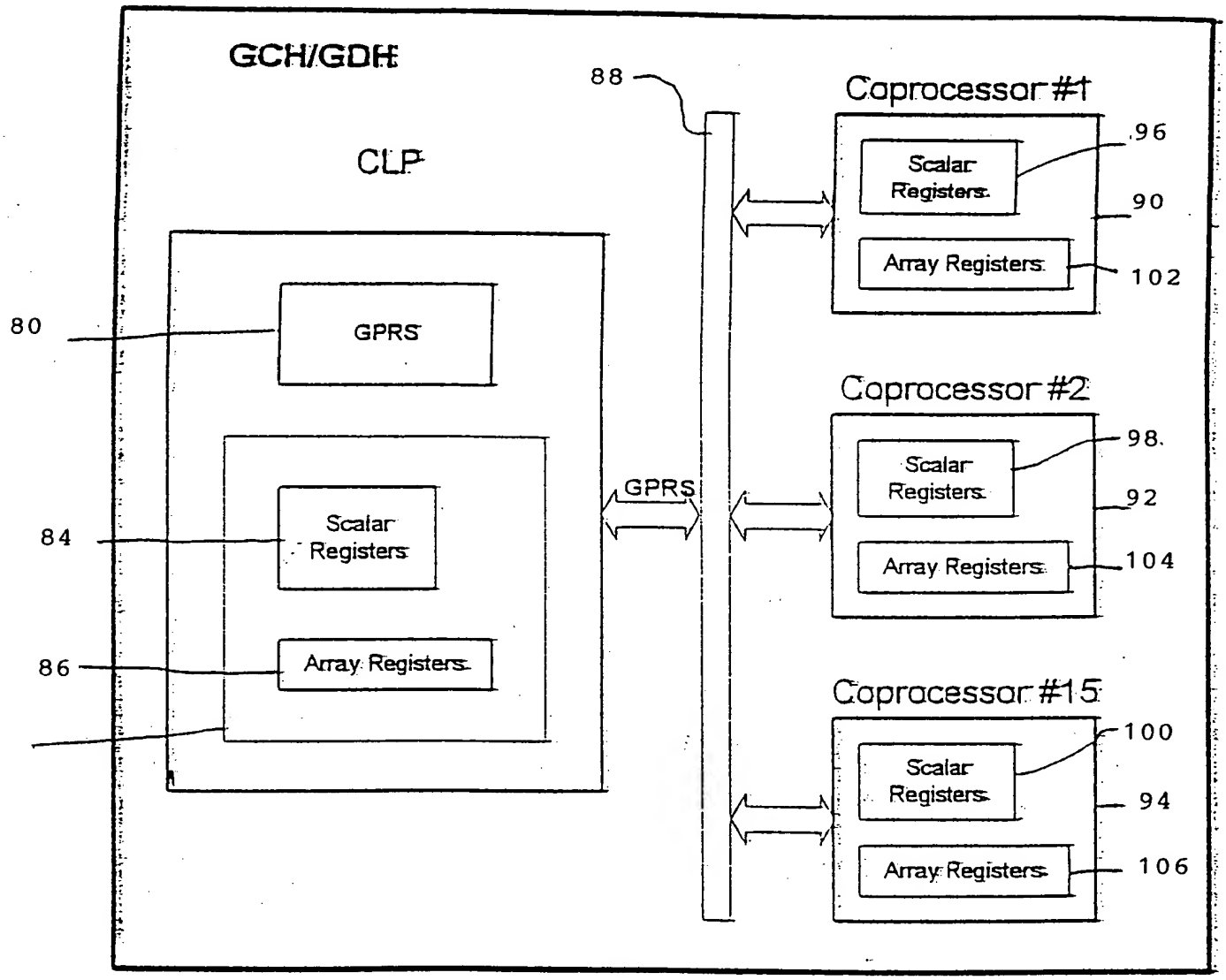
GCH/GDH
CLP
80
GPRS
84
Scalar Registers
86
Array Registers
82
88
GPRS
Coprocessor #1
Scalar Registers
96
90
Array Registers
102
Coprocessor #2
Scalar Registers
98
92
Array Registers
104
Coprocessor #15
Scalar Registers
100
94
Array Registers
106

FIGURE 3

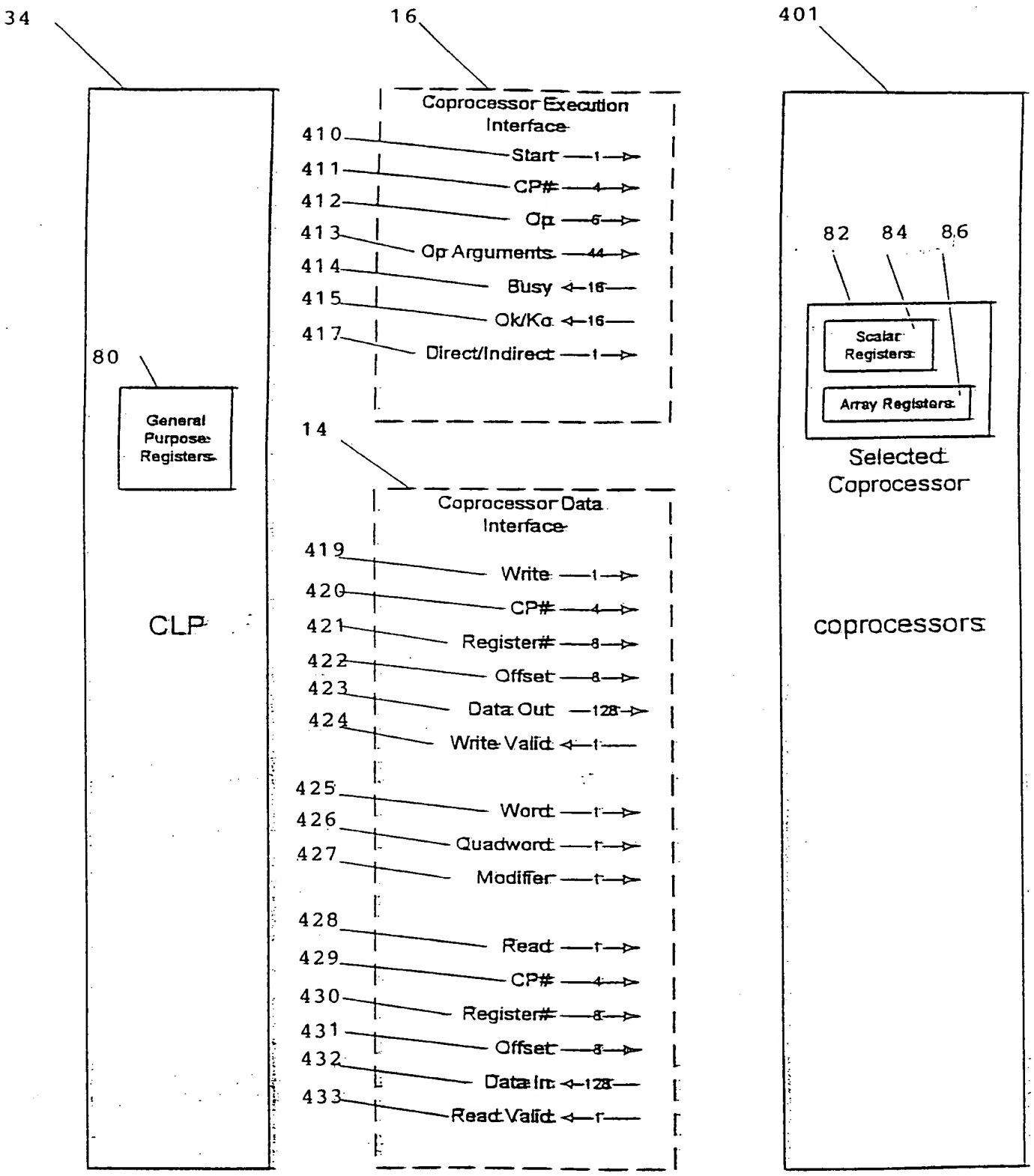
34
16
401
Coprocessor Execution Interface
410 Start 1
411 CP# 4
412 Op 6
413 Op Arguments 44
414 Busy 16
415 Ok/Ko 16
417 Direct/Indirect 1
80
General Purpose Registers
14
Coprocessor Data Interface
419 Write 1
420 CP# 4
421 Register# 8
422 Offset 8
423 Data Out 128
424 Write Valid 1
425 Word 1
426 Quadword 1
427 Modifier 1
428 Read 1
429 CP# 4
430 Register# 8
431 Offset 8
432 Data In 128
433 Read Valid 1
CLP
82 84 86
Scalar Registers
Array Registers
Selected Coprocessor
coprocessors

Figure 4

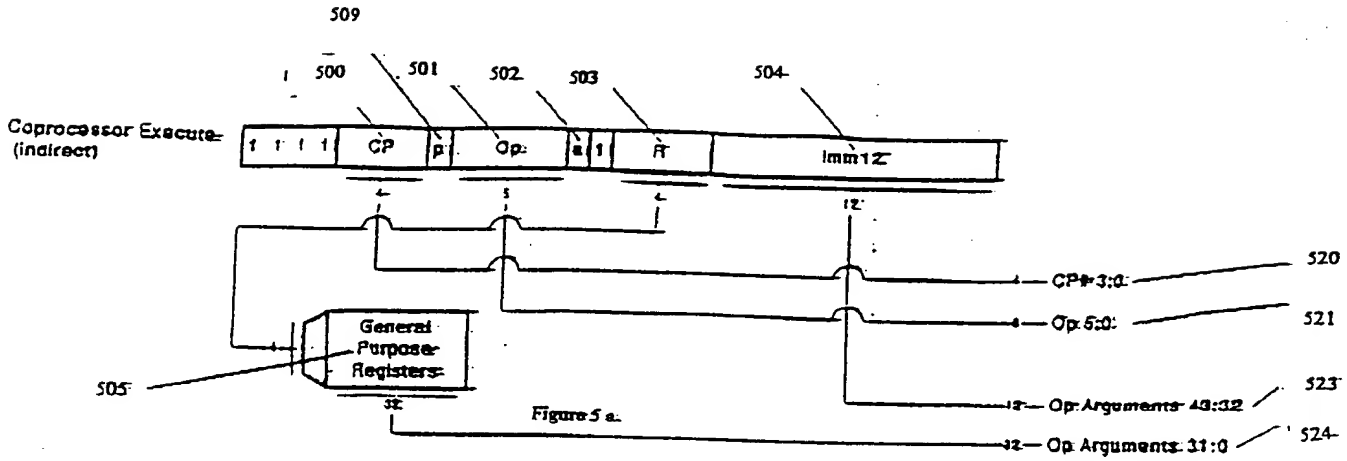

Figure 5 a.

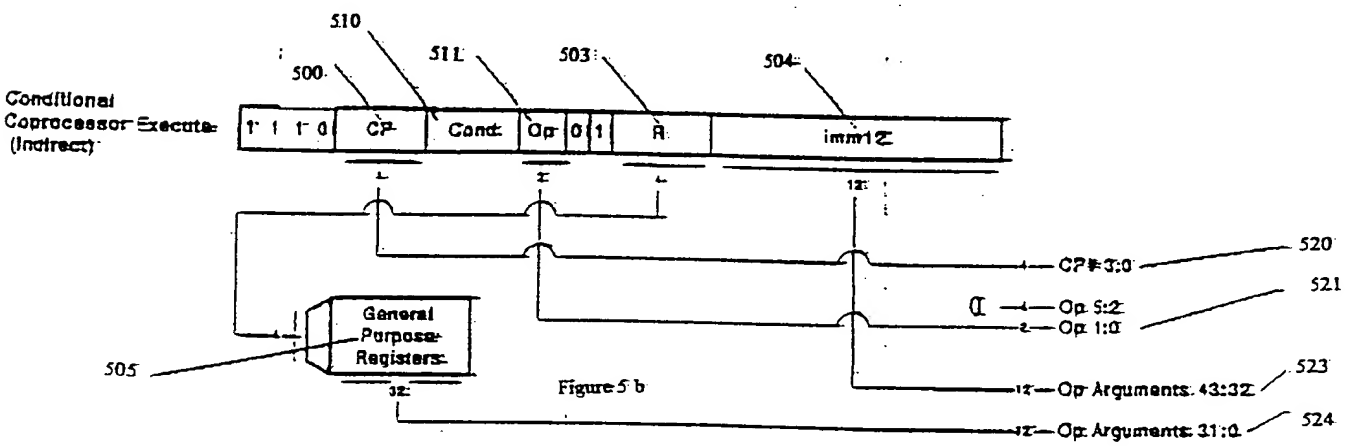

Figure 5 b

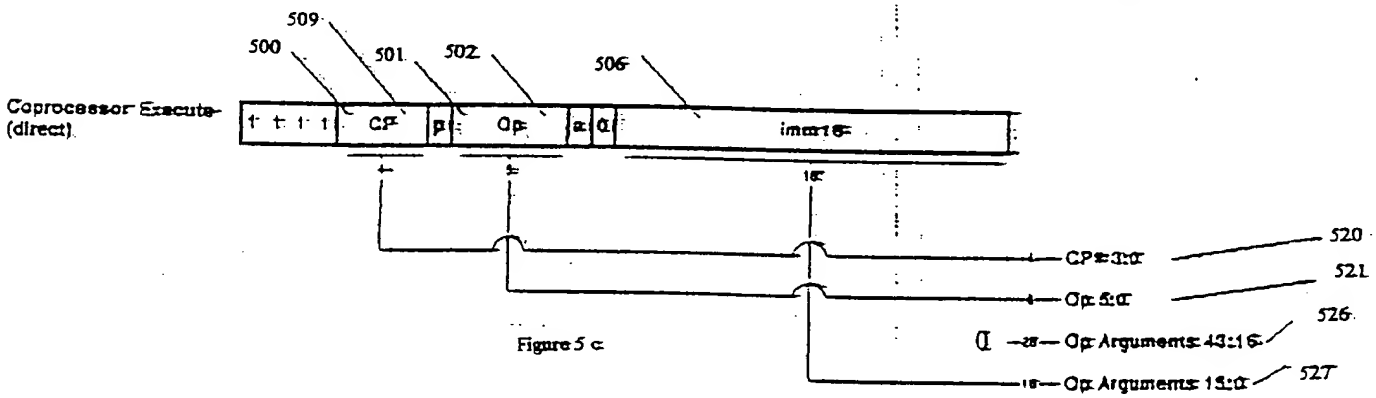

Figure 5 c

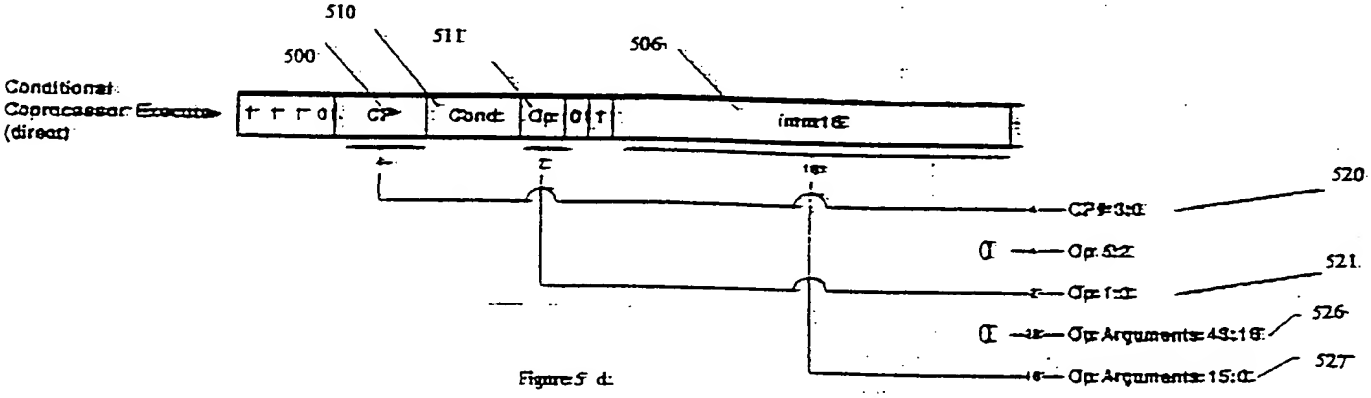

Figure 5 d.

Coprocessor Wait

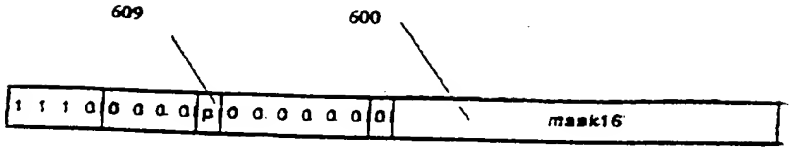

Figure 6 a

Coprocessor Wait and Branch

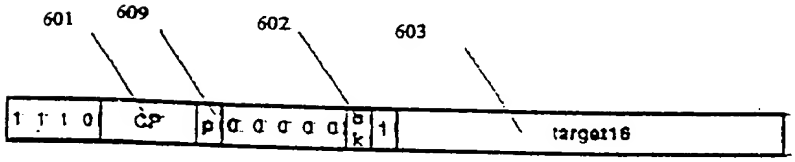

Figure 6 b